# AN746
Application Note

# A 3½ DIGIT DVM USING AN INTEGRATED CIRCUIT DUAL RAMP SYSTEM

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This application note describes the design of a 3½-digit DVM (digital voltmeter) using the MC1405 and the MC14435 dual ramp A/D system. The performance criteria is that of a lab quality DVM with both 3½-digit resolution and accuracy while still retaining a low cost and low parts count instrument. Features of the DVM include circuitry for a high impedance input, autopolarity and overrange indication.

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## INTRODUCTION

Motorola's MC1405 and the MC14435 combine to make a two chip A/D system that provides a very convenient and accurate building block for a 3½-digit DVM (digital voltmeter). The system consists of a linear subsystem (MC1405) providing the analog portion of the A/D and a CMOS subsystem (MC14435) providing the digital logic for the A/D. Together they provide an A/D package using the dual ramp technique of A/D conversion.

This note discusses a DVM designed around the two chip A/D system. The DVM features:

- 3½-Digit Resolution and Accuracy
- Autopolarity
- High Input Impedance
- Low Cost
- Low Package Count

## DUAL RAMP SYSTEM

There are many techniques of A/D conversion, each having different characteristics and each favoring different applications. The dual ramp technique of A/D conversion provides an inexpensive method of obtaining high accuracy which makes it ideal for DVM type applications. While a complete discussion of A/D techniques is beyond the scope of this note, a brief discussion of the dual ramp method will be helpful in understanding the circuit operation. Figure 1 shows a block diagram of the dual ramp system, while the basic dual ramp waveforms of these A/D techniques are shown in Figure 2.

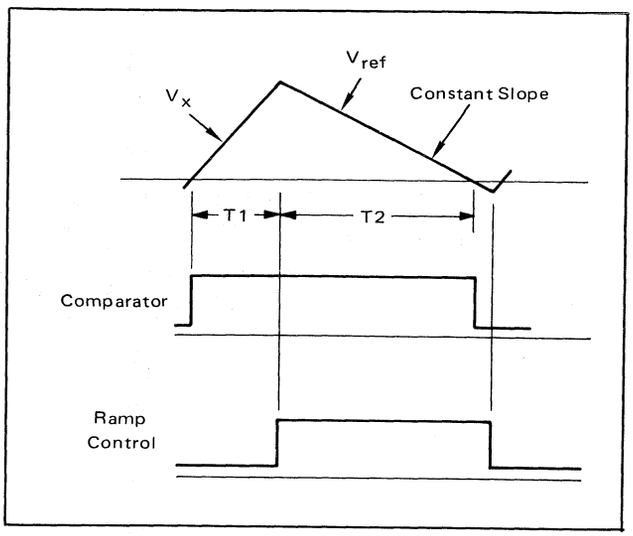


**FIGURE 2 – Dual Ramp A/D Converter Waveforms**

The dual ramp conversion cycle consists of two basic time periods. Time period T1 results from the input unknown voltage being integrated for a fixed time interval. This integration results in the output voltage of the integrator being proportional to the input unknown voltage. At the end of time period T1, the reference voltage ($V_{ref}$) is applied to the integrator, causing the integrator output voltage to decrease. This integration continues until the output voltage again reaches the zero reference level. This time interval, T2, is the down ramp time period.

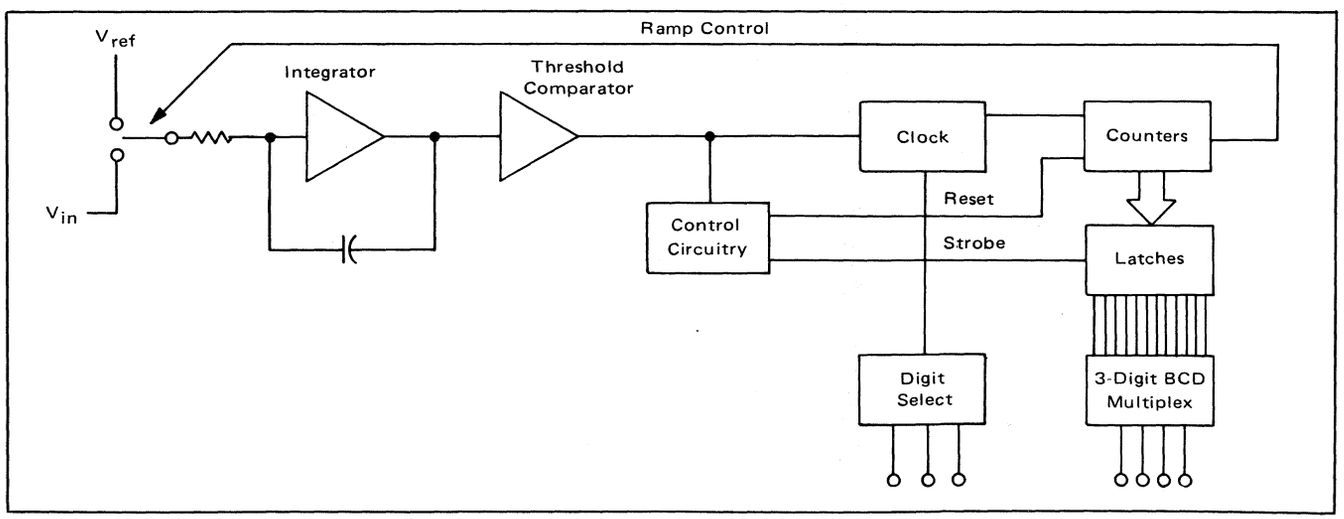


**FIGURE 1 – Dual Ramp Block Diagram**

Time period T1 is constant for each conversion cycle. The time interval T2 is dependent upon the input unknown voltage. Referring to the dual ramp waveform, it is apparent that:

$$\frac{T2}{T1} = \frac{V_X}{V_{ref}}$$

Looking at the four variables in this relationship, T1 is a fixed time period, T2 is measured from the start of the ramp-down time period until the zero level is reached, and $V_{ref}$ is calibrated into the system. The only remaining variable in the equation is $V_X$, which is the analog input to be determined. Thus by counting out a time period T1, measuring the down ramp time interval T2, and calibrating the reference voltage, the dual ramp A/D conversion technique determines the value of an analog input voltage.

This A/D conversion method also eliminates inaccuracies due to integrator capacitor drift and time or temperature drift in the clock frequency. These features result from the fact that the same integrator capacitor and the same clock frequency are used during both the up-ramp time period, T1, and the down-ramp time period T2. Thus if the clock frequency has drifted up 10% over some time period, both T1 and T2 will be 10% less, thus canceling the effect of the drift. Likewise, if the capacitor value drifts over time or temperature, the integrator voltage will be higher or lower at the end of T1 and at the beginning of T2. This again eliminates the errors due to a changing capacitor value.

### MC1405 and MC14435

As mentioned previously, the MC1405 and the MC14435 together produce a complete dual ramp A/D. The MC1405 is built with bipolar linear technology and the MC14435 is produced in CMOS digital processing. This allows the complete A/D system to be subdivided into blocks which allow mature processing technologies to be utilized in producing the A/D system.

The block diagram of the MC1405 is shown in Figure 3. The MC1405 contains the integrator required in this A/D technique as well as the analog switch required to switch between the unknown input and the reference voltage. Also included is the reference voltage, reference voltage to current converter, unknown voltage to current converter, and a comparator for the integrator output.

The selection of clock frequency and power supply voltage determines the integrating capacitor value. A polar capacitor may be used with pin 7 of the MC1405 connected to the + terminal. However, settling time will be increased if electrolytics are used. Tantalum electrolytics are preferred. The required capacitor can be calculated as follows:

$$C = I_{X(max)} \quad \frac{(\text{up ramp counts})(\text{clock period})}{V_{7(high_{min})} - V_{threshold(max)}}$$

For a 15 volt supply at 10 kHz and using MC14435,

$$0.7\ \text{mA}\ \frac{1000\ (100\ \mu s)}{(12.8 - 1.1)\ V} = 6\ \mu F$$

The ramp should be made as large as possible to achieve highest accuracy but should not be allowed to saturate the integrator in worst case conditions.

The MC14435 contains the counters and control circuitry of the 3½-digit dual ramp converter. This device has a 3½-digit BCD output with 3-digits multiplexed and the half digit unmultiplexed on a separate output pin. An

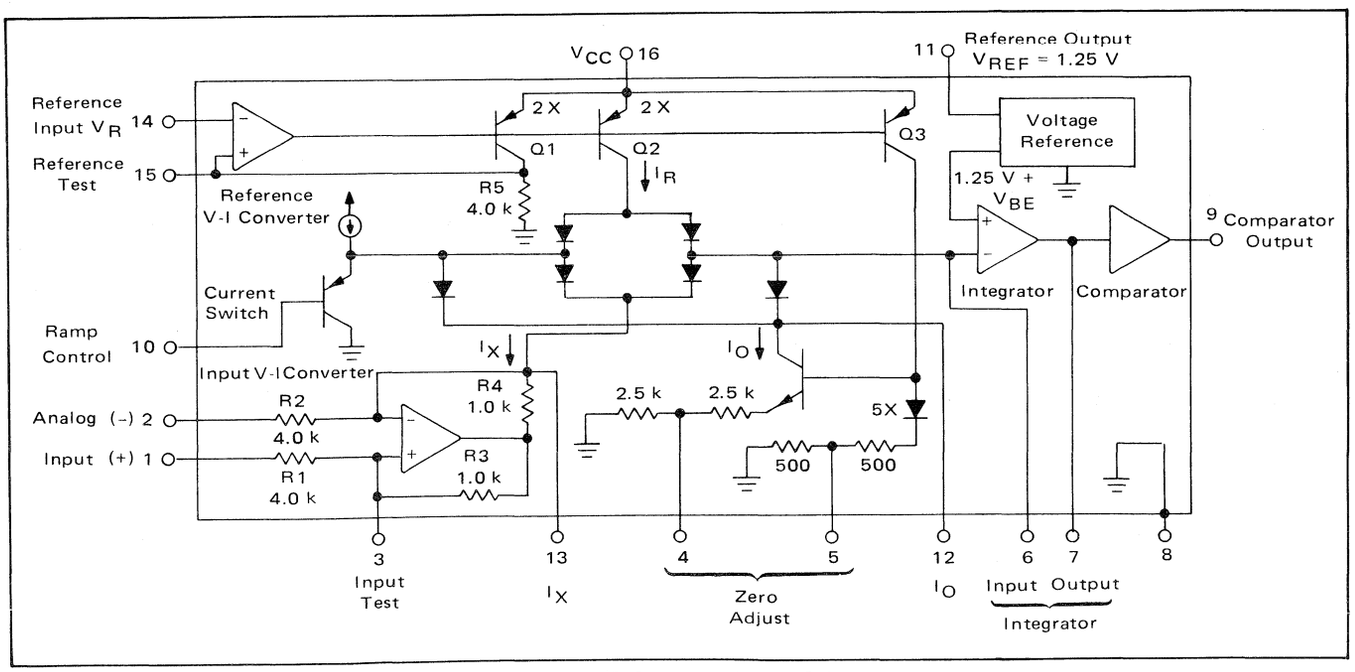


FIGURE 3 – A/D Converter Analog Subsystem

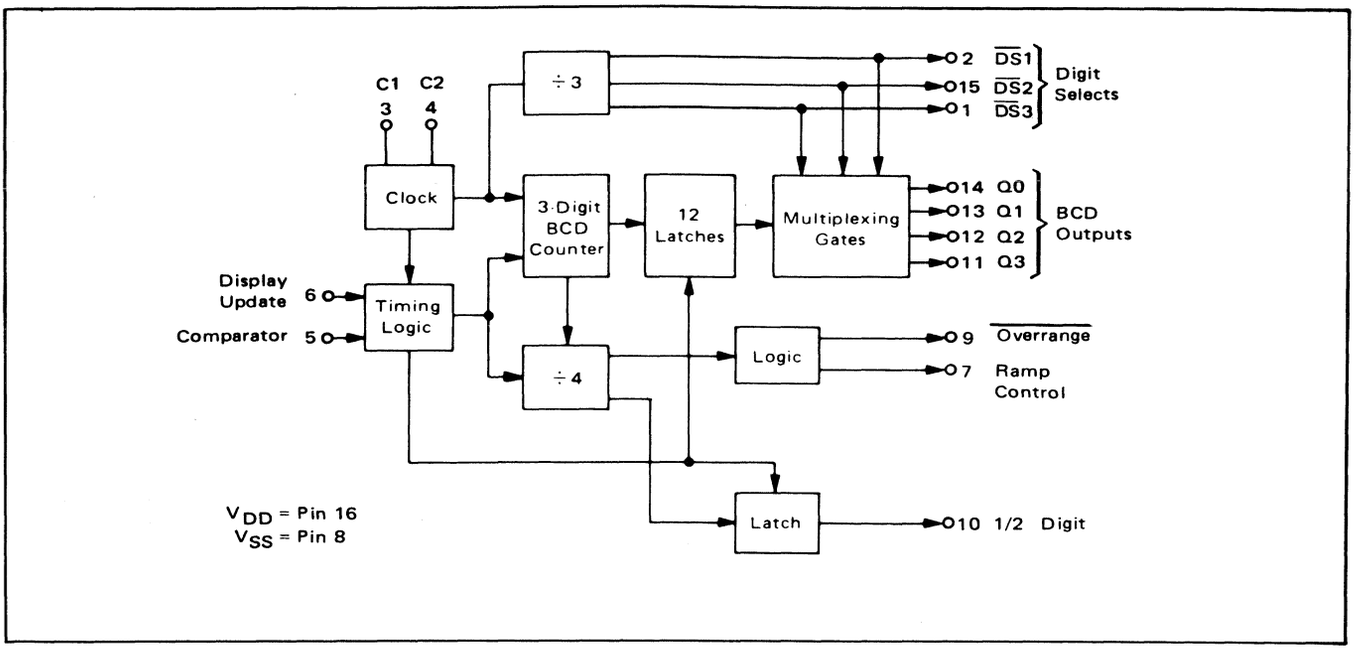


**FIGURE 4 – MC14435 Block Diagram**

overrange indication is provided as well as a display update pin which allows the data rate into the latches to be slowed or stopped. The multiplexed BCD outputs are normally low while the digit select lines are in a normally high state.

The clock capacitor across pins 3 and 4 of the MC14435 determines the frequency of the system clock. The oscillator frequency is dependent on the capacitor value, the operating voltage, and some process variations. The dual slope system may be operated from 1 kHz to 1 MHz depending on the application. A full scale conversion requires 3100 counts; thus up to 300 conversions per second are possible. However, when used to drive a display, such update rates are annoying to a viewer. Ten kHz is often chosen to provide about three conversions a second in visual display instruments. For 15-volt operation a clock frequency of 10 kHz is achieved with a 0.001 $\mu$F capacitor.

There are two connections between the MC1405 and the MC14435. The comparator output of the MC1405 indicates whether the integrator output is above or below the threshold level. The ramp control output from the MC14435 determines whether the input to the integrator is the unknown voltage or the reference voltage. At frequencies below 200 kHz an RC delay may be required on the output of the MC14435 ramp control. This time delay indirectly assures that the oscillator restarts (controlled by the comparator) are synchronized with each new conversion. At 10 kHz the delay should be sufficient to extend the comparator off time to 50 $\mu$s. That is one-half the period of the clock frequency. Ten k$\Omega$ and 0.01 $\mu$F will typically accomplish this.

In addition to the basic requirements for a dual ramp system, the MC1405 and MC14435 includes offset circuitry to stabilize voltage readings at or near zero. With the basic dual ramp system, near zero inputs will only charge the integrator capacitor to very small voltage levels. Then during the down ramp period, noise can cause the comparator to trigger prematurely, resulting in instability of the output display. By adding a constant current to the input of the integrator and subtracting out the number of clock pulses produced by this offset current, the Motorola dual ramp system never reaches the zero input conditions previously mentioned.

The two packages will operate from a single power supply between +5.0 and +15 volts. However, the DVM described here was designed for 15 volt operation and requires a negative voltage in addition to the positive supply voltage. This is used for the input and auto-polarity circuitry.

## DVM CIRCUIT DESCRIPTION

The complete DVM schematic is shown in Figure 5 and includes the digital readout, autopolarity circuit with indicator, high impedance input, and overrange indicator. There are 3 input voltage ranges that allow the DVM to measure a dc voltage of 0 – 1.999 V, 0 – 19.99 V and 0 – 199.9 V.

The basic A/D is constructed from the MC1405 and MC14435 as previously discussed. The MC1405 has two calibration potentiometers, R5 and R6. R5 sets the full scale calibration and R6 is used for zero adjust. Capacitor C2 is the integration capacitor and for 3½-digit continuous conversion, such as in this DVM, an electrolytic capacitor may be used. Capacitor C3 is added to the MC14435 to set the frequency for the internal oscillator. With the 0.001 $\mu$F value shown the clock frequency is about 10 kHz with a 15 V power supply.

The output of the DVM consists of the 3½-digit readout for voltage, polarity indication, and overrange indication.

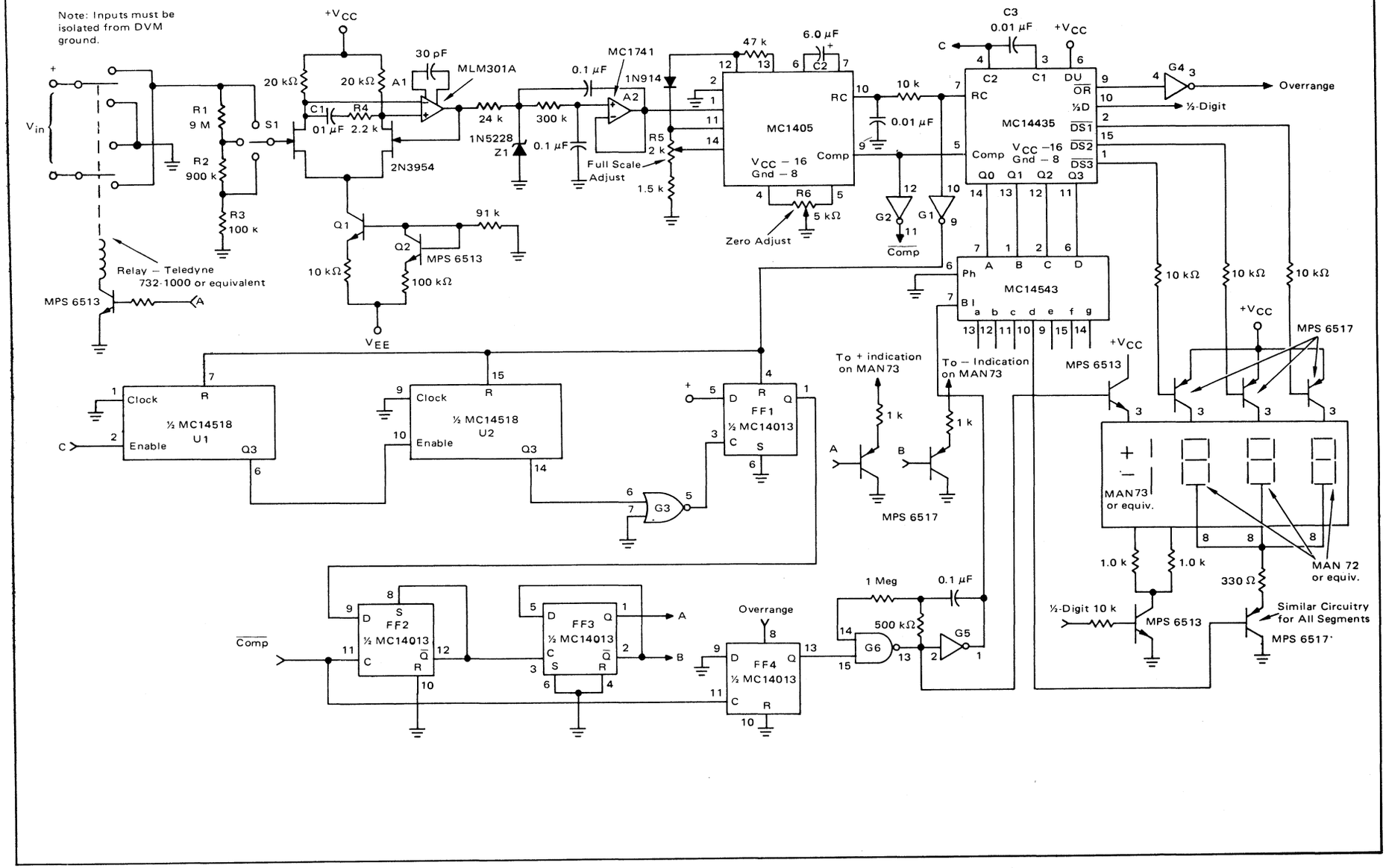


**FIGURE 5 – 3½-Digit DVM**

Seven-segment LED (Light Emitting Diode) displays are used for the 3 least significant digits of the display with a ½-digit display used to indicate both the ½-digit and the input polarity.

A single MC14543 seven-segment decoder is used to decode the multiplexed BCD digital output from the MC14435. By tieing the phase control (Pin 6) positive, the MC14543 will drive a common anode LED display such as is used in this DVM design. The outputs of the MC14543 are buffered with MPS6517 PNP transistors. The digit select outputs from the MC14435 are also buffered with PNP transistors. Each "ON" segment of the LED has an instantaneous current of about 30 mA or an average current of 10 mA due to the 30% duty cycle obtained when the LED's are multiplexed.

The internal operation of the MC14435 causes the half-digit to be blanked off until a voltage of 1.000 is reached. An NPN MPS6513 transistor is used to buffer the MC14435 output for the ½ digit display.

The plus and minus indicators are driven with PNP transistors from the CMOS autopolarity circuitry. This circuitry will be discussed later.

Although there are many methods to indicate that the input voltage has exceeded the allowable maximum, the method used here uses the overrange information from the MC14435 to blink the entire display ON and OFF at a 2 Hz rate. This condition occurs when the MC1405 input exceeds 1.999 volts. Flip-flop FF4 is used to latch the overrange information from the MC14435 and control a low frequency oscillator built from Gates G4, G5 and associated resistors and capacitors. The blanking control of the MC14543 is used for blinking the 3 full digits of the display while the half digit and polarity indicators are blinked via the MPS6513 NPN transistor in the anode of the ½ digit display.

The remaining circuits in the DVM schematic of Figure 5 perform the high impedance buffering and autopolarity for the MC1405.

## INPUT BUFFER CIRCUITS

The MC1405 has a low impedance input (typically 4K) which in many applications must be buffered to minimize the loading effect on the circuit being evaluated. An operational amplifier may be used as a buffer. However, the op amp does require a sizable bias current that must be supplied by the voltage source under test. This fact makes the simple operational amplifier undesirable for general purpose DVM applications.

Higher input impedances with lower bias currents than that of a bipolar operational amplifier can be obtained by using a FET input in front of the op amp. A single JFET operated as a source follower can be used if the JFET is compensated at the zero drift point, however, this is time consuming and expensive to do in production quantities. A differential stage built from discrete FET's would have temperature drift characteristics inconsistent with the precision of the MC1405.

Monolithic FET input operational amplifiers with drift characteristics that are compatible with the accuracy of the MC1405 are usually quite expensive. By using matched dual FET's in conjunction with a bipolar op amp, the desired drift characteristics may be maintained while achieving an economical design.

The high input impedance buffer shown in the DVM schematic consists of the 2N3954 dual FET and an MLM301A bipolar operational amplifier. The overall amplifier has a high input impedance and operation as a voltage follower assures an accurate closed loop gain from the amplifier.

The input impedance of the amplifier is 10 MΩ which is set by the input voltage divider R1, R2 and R3. The FETs are connected as a differential amplifier with the source leads common and returned to a constant current generator. This constant current source is bipolar transistor Q1 with temperature compensation by a second similar transistor, Q2, to match the $V_{BE}$ drifts of Q1. The drain current will be about 350 $\mu$A and the drain voltage about 7 volts with a ±15 volt power supply.

The op amp chosen was an MLM301A, compensated with a 30 pF capacitor. Additional compensation for loop stability is done with the resistor/capacitor network R4 and C1. The temperature drift of this amplifier is typically well under 1 mV for a temperature range from 0°C to 50°C.

Switch S1 is used to select the maximum input voltage range of the DVM. These ranges are 1.999 V in 1 mV increments, 19.99 volts in 10 mV increments and 199.9 volts in 100 mV increments. Resistors R1, R2 and R3 should be matched to better than .05% or each could be trimmed with a small series trimpot. Zener diode, Z1, which follows amplifier A1, is used to protect the MC1405 if a voltage greater than 5.0 volts is accidently applied to the input of the 2N3954.

Amplifier A2 and associated components produce a Sallen and Key complex pole low pass filter. This filter helps reduce 60 Hz signals that are picked up when resistance is placed between the signal source and the DVM ground. With the component values shown, the filter has a corner frequency of 6.0 Hz, a damping factor of 0.6 and a gain of 1.0. With this design the 60 Hz amplitude is reduced by 40 dB at the MC1405 input. Small-gain and offset errors from the input stages can be calibrated out with the existing full scale and zero adjustments of the MC1405.

## AUTOPOLARITY

Autopolarity, or the ability to handle both positive and negative input voltages, is accomplished by switching the inputs with a mechanical relay to always provide a positive input to the MC1405.

This technique is simple but has the disadvantage of requiring either the inputs to the relay or the inputs to the MC1405 to be isolated from the DVM ground reference. However, if the MC1405 inputs were allowed to float and ground reference was established at the input of the relay, reversal of the polarity switch would result in a common

mode level shift at the MC1405 input which will affect the calibration of the unit. Therefore, the input voltage must be allowed to float with respect to the MC1405 ground reference.

In order to detect the polarity of the input voltage and control the relay to always maintain a positive polarity to the input of the MC1405, a digital polarity detection scheme is used. The digital polarity detector has the advantage over analog techniques of not requiring any additional offset adjustment or temperature tracking. Polarity detection is accomplished by using the comparator output of the MC1405 in conjunction with the MC14435 digital subsystem.

As mentioned previously, the MC1405 adds an offset current during the reference integration. In the case of a 3½-digit DVM, a 100 count offset is produced which is subtracted out in the digital subsystem. If the input polarity is positive or zero, there are at least 100 clock pulses coming from the MC14435 clock. However, if the input polarity is negative the unknown current is subtracted from the offset current and less than 100 clock pulses are gated into the counters. This fact can be used to determine the input polarity.

The number of counts may be determined by the first two stages of the counter chain in the digital subsystem, however, since these are not available externally to the MC14435, MC14518 dual BCD counters are used. Referring again to Figure 5, the MC14518 (U1, U2) counter output is fed into a D flip-flop, FF1, which toggles the Q output high when 100 counts have come from the clock. This information is latched into FF2, holding Q low, when the comparator output from the MC1405 goes low indicating the end of a conversion cycle. This output does not toggle FF3, and the relay does not change position. However, when the input polarity is reversed, FF1 will not have been toggled high when the comparator goes low. This causes FF2 $\overline{Q}$ to momentarily go high, toggling FF3 and reversing the position of the relay. Thus, after completing a conversion cycle with a negative input voltage to the MC1405, the relay is toggled to apply a positive voltage to the MC1405 which can be measured. Diode D1 on the MC1405 is used for recovery from negative differential input voltages. A 47 kΩ resistor between pins 12 and 13 is used to insure that negative inputs do not latch the comparator low before the relay is reversed.

## CALIBRATION

DVM calibration only requires adjustment of the two potentiometers on the MC1405. The calibration first consists of shorting the input leads together and adjusting the zero calibration potentiometer, R6, until the display reads zero. Adjusting the zero calibration potentiometer slightly negative will cause the display to toggle between plus and minus polarity.

Full scale calibration with R5 requires an accurate reference to be applied to the DVM input. For best accuracy, the value of this reference should be as close to full scale as possible on the direct input, or in this case 1.999 volts. If the voltage divider resistors R1, R2, R3 consist of trimpots then each of the three input voltage ranges must also be adjusted.

For additional information on Motorola's A/D system, consult the following publications:

1. MC1405 Data Sheet
2. MC14435 Data Sheet
3. EB 24 – Input Buffer Circuits for the MC1505 Dual Ramp A/D Converter Subsystem
4. EB 35 – Autopolarity Circuits for the MC1505 Dual Ramp A/D Converter Subsystem
5. EB 36 – A 4½-Digit DVM System Using the MC1505
6. EB 50 – A Simple Battery Powered 3½-Digit DVM.
7. EB 55 – A Battery Powered 3½-Digit Digital Multimeter.
8. AN-748 – Applications of the MC1405/MC14435 in Digital Meters.

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